# Charge-Domain Leaky-Integrate-and-Fire Neuron with Tunable Parameters Using Ferroelectric Non-Volatile Capacitors

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## Abstract

This work presents a charge-domain leaky-integrate-and-fire (LIF) neuron circuit that leverages ferroelectric non-volatile capacitors (nvCAPs) to achieve multiple tunable parameters for enhanced configurability in spiking neural networks (SNNs). Key to its innovation is the use of nvCAPs not merely as non-volatile storage, but as primitives shaping neural dynamics and communication by controlling (i) membrane dynamics, (ii) refractory period, and (iii) synaptic output weight. Unlike current-domain neurons, the proposed architecture emits spikes as quantized charge packets, enabling weighted distribution to multiple downstream nodes with negligible static output power. We demonstrate the neuron's functionality with circuit simulations in a 28-nm CMOS process using experimentally calibrated nvCAP models, showing how nvCAP programming alters the membrane time constant and spike magnitude. A speed-adaptable SNN classification study on the UCI-HAR dataset demonstrates that programmable membrane time constants can preserve classification performance across varying input temporal scales without retraining. Benchmarking against prior LIF neuron implementations shows that the proposed design provides a balanced combination of compactness, low spike energy, and multi-parameter programmability while uniquely integrating charge-domain operation with non-volatile neuron tuning. This work establishes a pathway toward reconfigurable and energy-efficient neuromorphic hardware by embedding non-volatile memory elements directly into the core analog dynamics of the spiking neuron.

## Keywords

leaky-integrate-and-fire neuron, spiking neural networks, ferroelectric capacitor, charge-domain computing, neuromorphic

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## 1 Introduction

Spiking Neural Networks (SNNs) have emerged as a prominent neuromorphic computing paradigm, distinguished by their potential for ultra-low-power operation and their close imitation of biological neural processes [16]. Unlike conventional artificial neural networks (ANNs) that rely on continuous-valued signals, SNNs encode information temporally through sparse, event-driven spike trains. From a hardware perspective, this temporal sparsity can translate into high energy efficiency, as energy consumption is concentrated in spike events while inactive periods incur only minimal background activity. Furthermore, analog implementations of SNNs can be advantageous because they leverage the intrinsic physical dynamics of electronic devices to process spike-based signals, improving energy efficiency compared to digital implementations [8, 9]. Consequently, SNNs represent a compelling alternative for deploying neural network capabilities in size-weight and power (SWaP) constrained edge computing applications.

At the core of many SNN models is the leaky integrate-and-fire (LIF) neuron, a simplified abstraction of biological neuronal dynamics that captures how cells integrate synaptic inputs and generate spikes over time. In the LIF formalism, inspired by Lapicque's integrator model [12] and later refined in modern computational neuroscience, the neuron is modeled as a single-compartment effective RC membrane whose voltage $v(t)$ obeys

$$\begin{aligned} \tau_{\mathrm{m}} \frac{dv_j}{dt} &= ((v_{\mathrm{leak}} - v_j) + R_{\mathrm{lk}} I_{\mathrm{syn}}(t)) * (r_j(t) \le r_{\mathrm{ref,th}}) \\ \frac{dr_j(t)}{dt} &= -r_j(t), \quad s_j(t) = 0, \quad \tau_m = R_{\mathrm{lk}} C_{\mathrm{st}} \end{aligned} \tag{1}$$

With the explicit spiking and reset mechanism:

$$v_j(t) \ge V_{\mathrm{thresh}} \rightarrow \begin{cases} v_j(t) = V_{reset} \\ s_j(t) = 1 \\ r_j(t) = t_{ref} \end{cases} \tag{2}$$

which defines the LIF neuron dynamics with explicit refractory gating. Here, $\tau_{\mathrm{m}}$ is the membrane time constant, $v_{\mathrm{leak}}$ is the leak potential, $v_j(t)$ is the membrane voltage of neuron $j$, $I_{\mathrm{syn}}(t)$ is the synaptic input, $R_{\mathrm{lk}}$ is the membrane leakage resistance, and $C_{\mathrm{st}}$ is the membrane capacitance. A spike output variable $s_j(t)$ is defined as a binary indicator that is set to 1 when the neuron fires and 0 otherwise. A refractory state variable $r_j(t)$ is introduced, decaying as $\frac{dr_j}{dt} = -r_j$, and gating integration through the condition $(r_j(t) \le r_{\mathrm{ref,th}})$, where $r_{\mathrm{ref,th}}$ is a finite recovery threshold. When $v_j(t) \ge V_{\mathrm{thresh}}$, a spike is emitted, the membrane resets to $V_{\mathrm{reset}}$, and $r_j(t)$ is set to $t_{\mathrm{ref}}$.

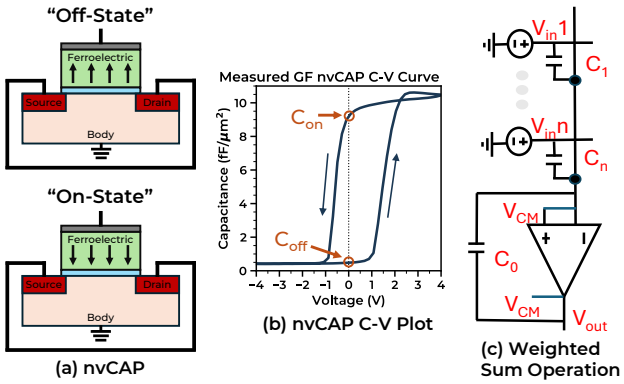



**Figure 1: (a) GlobalFoundries FeFET configured as an nvCAP. Off-state: upward dipole orientation with low capacitance. On-state: downward dipole orientation with high capacitance. (b) Measured C–V curve of a 3.33 $\mu$m × 3.33 $\mu$m nvCAP device. (c) Two-stage weighted-sum operation.**

## 2 Charge-Domain Computing

The deployment of neural networks (NNs) on edge devices is limited by strict energy constraints. To address this, compute in memory (CIM) architectures have emerged to accelerate vector–matrix operations, typically using crossbar arrays [6, 21]. However, current domain CIM suffers from high static power when synaptic resistances are low (kΩ range). Prior works [10, 11, 23] have addressed this limitation using ferroelectric non volatile capacitors (nvCAPs), which enable transient charge transfer and eliminate static power consumption. In this work, the nvCAP is implemented using the GlobalFoundries 28 nm FeFET platform [3].

When configured in nvCAP mode, ferroelectric polarization modulates the channel charge distribution, producing distinct low and high capacitance states (LCS and HCS) through C–V asymmetry in a non destructive read operation, with an on/off capacitance ratio of approximately 25 at 0 V bias (Fig. 1a–b). This behavior arises from polarization dependent modulation of the FeFET channel: downward dipoles (HCS) promote channel inversion and increase capacitance, while upward dipoles (LCS) suppress inversion and reduce capacitance.

The weighted sum operation shown in Fig. 1c illustrates the principle of charge domain computation via charge transfer: input voltages charge synaptic capacitors, and the stored charge is then released as charge packets, i.e., discrete amounts of charge $\Delta Q = C_w V_{\text{in},i}$ from each weighted capacitor, to an output node, producing a voltage proportional to the weighted sum.

## 3 Proposed Neuron Design

### 3.1 Neuron Design

The proposed charge-domain neuron implements leaky-integrate-and-fire (LIF) dynamics using four mixed-signal blocks shown in Fig. 2a: (1) an input charge accumulator node with a leak, (2) a pull-down reset network, (3) a threshold detector comparator, and (4) a charge-packet generator. In the schematic, $V_{\text{mem}}$ is the membrane node; $C_{\text{st}}$ is the membrane capacitor implemented with nvCAP;

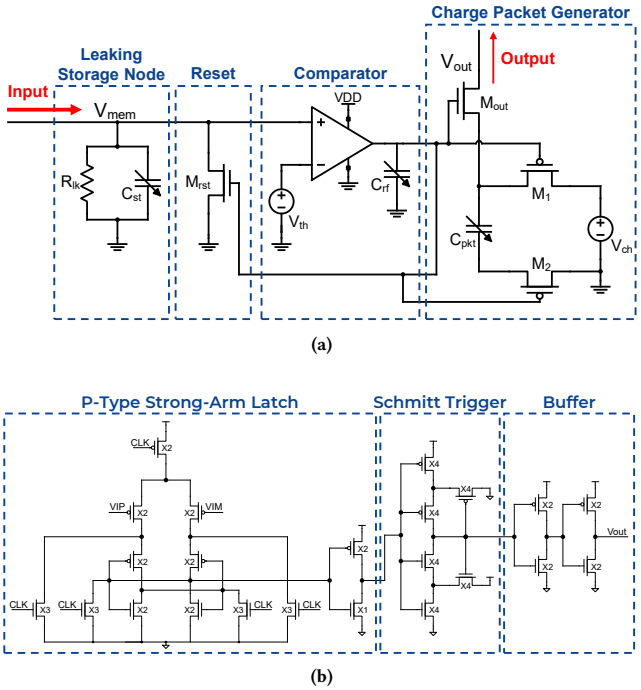



**Figure 2: (a) Proposed charge-domain LIF neuron top-level schematic. (b) Comparator schematic.**

$R_{\text{lk}}$ is the leakage path from $V_{\text{mem}}$, which can be realized using either a physical resistor or a MOS transistor biased in subthreshold; $M_{\text{rst}}$ is the pull-down transistor; $V_{\text{th}}$ is the firing threshold voltage; $C_{\text{rf}}$ sets the refractory timing; $C_{\text{pkt}}$ is the output packet capacitor; $V_{\text{ch}}$ is the pre-charge voltage for $C_{\text{pkt}}$, $M_1$ and $M_2$ are the charging switches for the charge packet generator; and $M_{\text{out}}$ is the output switch that releases the charge packet during a fire. All circuit design and simulation were performed in the GlobalFoundries 28 nm foundry process-design-kit (PDK)[3], with experimentally calibrated Verilog-A macromodels used to represent the nvCAP device in circuit simulations.

The operation of the circuit is as follows: The membrane node $V_{\text{mem}}$ accumulates input charge packets and collects the charge on the membrane capacitor $C_{\text{st}}$. Charge leaks through $R_{\text{lk}}$ while the membrane voltage is below the voltage threshold. The op-amp comparator circuit detects when $V_{\text{mem}}$ crosses the voltage threshold $V_{\text{th}}$ and initiates the output firing by raising its output signal. When this occurs, the charge-packet generator releases the output charge packet and the pull-down transistor turns on, discharging $V_{\text{mem}}$ toward 0 V to reset the membrane. The membrane reset completes as $V_{\text{mem}}$ reaches 0 V and the comparator output returns to 0 V. The high-time of the comparator (set by the reset path and $C_{\text{rf}}$) defines a hard refractory period during which integration and new spikes are prohibited.

### 3.2 Comparator Design

To implement the comparator functionality within the neuron, a three-stage architecture is adopted, consisting of a P-type strong-arm comparator, a Schmitt trigger, and an output buffer as shown

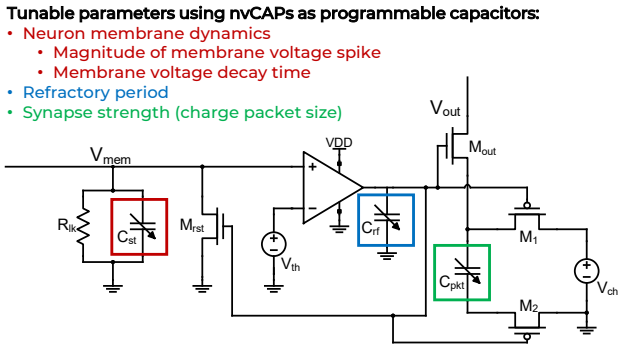



**Figure 3: The nvCAP can be implemented as the three internal capacitors in order to control neuron parameters: 1. Neuron membrane dynamics (magnitude of membrane spikes and decay rates), 2. Refractory period, and 3. Synaptic strength (output charge packet size).**

in Fig. 2b. The strong-arm comparator employs PMOS input transistors to enable reliable sensing under low input voltage conditions while avoiding subthreshold operation of the input devices, which would otherwise degrade the comparison speed. Furthermore, global or local clock-controlled operation significantly reduces power consumption compared to continuous-time amplifiers.

The Schmitt trigger introduces hysteresis to stabilize the comparator output. When $V_{IP} > V_{IM}$, the output $V_{OUT}$ switches to logic '1', activating the pull-down transistor $M_{pd}$ to discharge the $V_{mem}$ node. Conversely, when $V_{IP} < V_{IM}$, $V_{OUT}$ does not immediately transition to '0', allowing $M_{pd}$ to remain on sufficiently long to fully discharge $V_{mem}$. The discharge duration can be precisely controlled by tuning the device dimensions of the Schmitt trigger.

To further reduce power consumption, a low supply voltage is employed for both the comparator and the Schmitt trigger. An additional output buffer operating at a higher supply voltage is incorporated to restore signal levels and provide sufficient drive capability for subsequent stages.

## 4 Tunable parameters using nvCAPs

We propose using the nvCAP device in three locations to make the neuron's parameters and firing behavior tunable to user requirements. In this implementation, the capacitance of each device can be dynamically programmed during operation. Each nvCAP can be set to a high- or low-capacitance state, which directly affects the RC time constants of key nodes in the circuit. Fig. 3 illustrates the three roles of the nvCAP devices in the proposed LIF neuron: neuron membrane dynamics, refractory period, and synaptic strength.

### 4.1 Neuron Membrane Dynamics

Utilizing the nvCAP device as the membrane capacitor $C_{st}$ allows tuning of the dynamics of the membrane node. When the nvCAP is put in the off-state, the neuron becomes more sensitive to input charge packets because less charge is required to reach the membrane-voltage threshold for firing. By the charge relation $Q = CV$, the reduced capacitance in the off-state produces a larger change in membrane voltage for a given input charge. Conversely, programming the nvCAP to the on-state makes the neuron less sensitive, since a larger amount of input charge is required to reach threshold.

Programming the nvCAP also sets the membrane decay time constant, $\tau = R_{lk}C_{st}$, and thus the neuron's effective time scale. Fig. 4 illustrates this by comparing both capacitance states. In Fig. 4a, small, high-frequency input charge packets (100 $\mu$s spacing) are applied: the off-state ($C_{st}$ = 50 fF, $R_{lk}$ = 10 G$\Omega$) reaches threshold, while the on-state ($C_{st}$ = 1.25 pF) remains subthreshold. In Fig. 4b, larger, lower-frequency input charge packets (**2.5** ms spacing) are applied: the off-state spikes after each input, while the on-state spikes less frequently due to its larger capacitance and longer time constant. This example corresponds to a nvCAP with on/off ratio of 25, consistent with measured GlobalFoundries devices (Fig. 1b). The evenly spaced input packets shown are for illustration only; the neuron does not require fixed-rate inputs. This enables temporal encoding via the relative arrival times of input charge packets.

Prior work has explored modulation of neuron time constants as a mechanism for improving temporal processing in spiking neural networks. For example, [5] proposed the Parametric Leaky Integrate-and-Fire (PLIF) neuron, in which the membrane time constant is treated as a trainable parameter and optimized through backpropagation together with the synaptic weights. Biologically inspired adaptive spiking neuron models have also been proposed, where additional internal state variables dynamically modify neuron excitability during network operation to improve performance on temporal tasks [1]. More recent work has extended this concept to inference-time adaptation, where neuron parameters such as the effective leak (and corresponding time constant) are modulated during operation through context-dependent control signals [13]. While these approaches demonstrate the benefits of dynamic neuron parameters, they rely on continuous runtime modulation of neuron dynamics. In contrast, the proposed method enables post-training temporal adaptation directly in hardware through programmable nvCAP device states, allowing the neuron time constant to be reconfigured during inference without retraining or continuous control signals.

## Application: Speed-Adaptable SNN Classification

To demonstrate the utility of the reconfigurable time constants discussed above, we consider a task involving real-world time-series signals which exhibit variability in their temporal scale. For example, the same human activity may be performed faster or slower depending on the individual or context. Conventional SNNs typically use neurons with fixed membrane time constants, meaning the network is implicitly tuned to a particular temporal scale during training. When the input sequence occurs faster or slower than the training conditions, the effective temporal dynamics of the neuron change relative to the signal, leading to degraded classification performance. The programmable membrane capacitance provided by the nvCAP enables dynamic adjustment of the neuron membrane time constant $\tau$, allowing the network to compensate for such variations in input speed.

To demonstrate this capability, we implemented a speed-adaptation experiment using the UCI Human Activity Recognition (UCI-HAR) dataset. This dataset contains six activity classes (walking, walking upstairs, walking downstairs, sitting, standing, and laying) derived from smartphone inertial sensor measurements. Each input sample

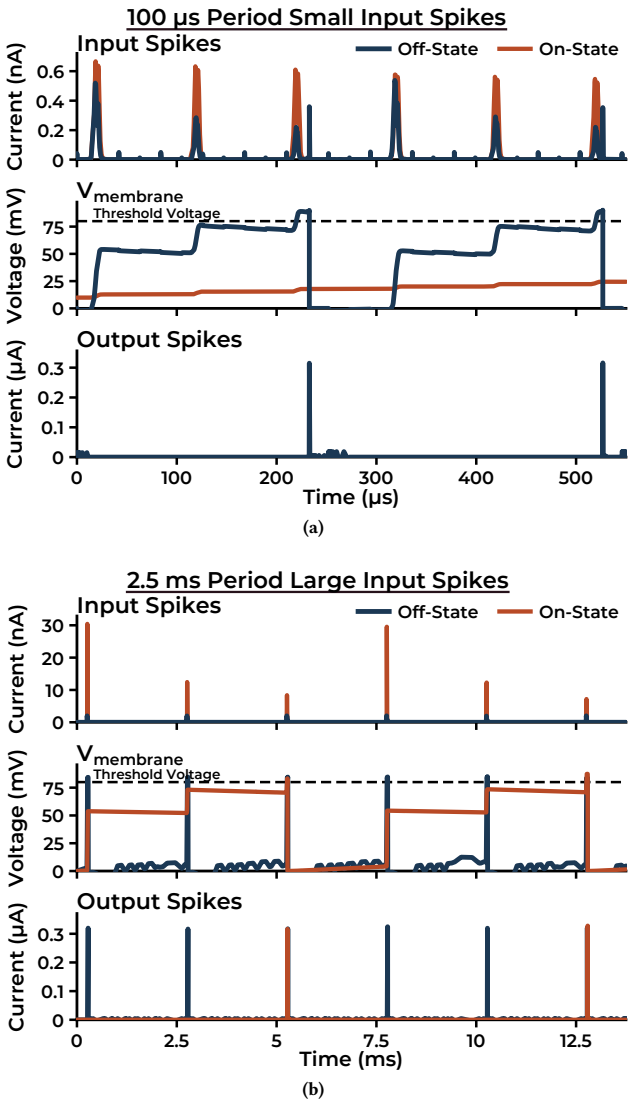



**Figure 4: The neuron's membrane node decay rate varies with the state of the nvCAP used as $C_{st}$. This example uses an on/off capacitance ratio of 25, with $C_{off} = 50\,fF$ and $C_{on} = 1.25\,pF$, and $R_{lk} = 10\,G\Omega$. (a) Small, high-frequency input charge packets (100 $\mu s$). The off-state reaches threshold, while the on-state remains subthreshold. At this timescale, comparator switching introduces minor transient artifacts on the waveform. (b) Larger, lower-frequency input charge packets (2.5 ms). The off-state spikes after each input, while the on-state spikes less frequently.**

consists of a multichannel time series of accelerometer and gyroscope data. The signals were processed as fixed-length temporal windows and presented to a fully connected SNN with architecture 9 input neurons, two hidden layers of 512 LIF neurons each, and a six-class readout layer. The network was trained at a nominal time scale, corresponding to a fixed simulation timestep $\Delta t$, using a constant membrane time constant during training.

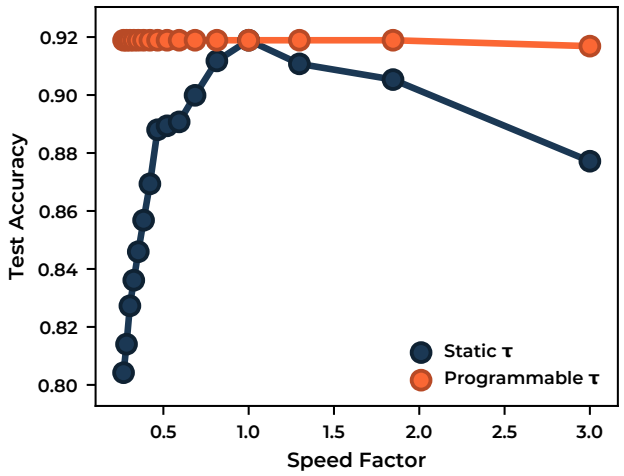
To emulate temporal variations in activity speed, the same input sequences were evaluated at different speed factors $s$, implemented by scaling the effective timestep of the neuron dynamics. Specifically, a faster input sequence corresponds to a smaller effective timestep $\Delta t_{eff} = \Delta t/s$, which changes the effective integration behavior of the neuron. In a conventional SNN with fixed $\tau$, this temporal scaling disrupts the relationship between spike integration and input timing, reducing classification accuracy as the input speed deviates from the training condition (Fig. 5a).

In contrast, the proposed programmable-capacitance neuron allows the membrane time constant to be adjusted according to the input speed. During inference, $\tau$ is selected according to an inverse scaling rule $\tau(s) \approx \tau_0/s$, where $\tau_0$ is the optimal time constant determined at the nominal speed. In the simulations, the nvCAP membrane capacitor is modeled with 16 discrete programmable states, producing membrane time constants linearly spaced from 14 ms to 168 ms (approximately a 12× range). This range remains within the assumed hardware capability of the nvCAP device while reducing quantization artifacts across the evaluated speed range. The desired $\tau$ value computed from the inverse-speed rule is then snapped to the nearest programmable state, representing the discrete capacitance levels available in hardware (Fig. 5b). Prior work has demonstrated multi-level programmability in ferroelectric memcapacitors and nvCAP devices [7, 14], suggesting that the 16 states could be realized through a small binary-weighted nvCAP bank ($2^n$ states from $n$ devices) or a single multi-state device, although reliable multi-state operation remains an active research topic.

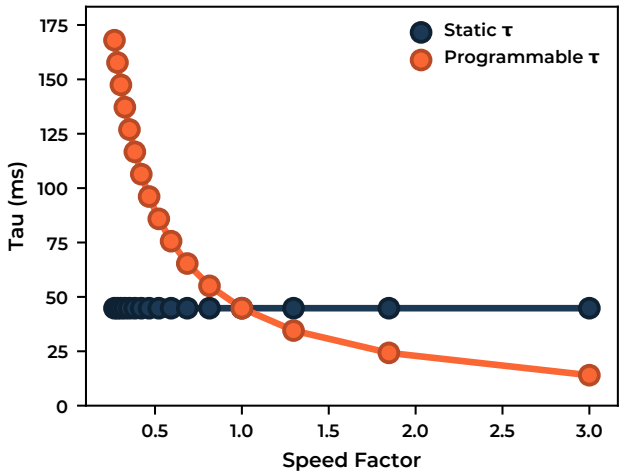
Fig. 5a shows the resulting classification accuracy as a function of speed factor for both the fixed-$\tau$ baseline and the programmable-$\tau$ approach across the full six-class dataset. While the baseline network experiences increasing accuracy degradation as the input speed deviates from the training condition, the programmable-$\tau$ network maintains nearly constant performance across the evaluated speed range. Fig. 5b illustrates the corresponding selected $\tau$ values versus speed factor, demonstrating the inverse relationship between the neuron time constant and the input temporal scale. These results highlight how programmable membrane capacitance allows the network time constants to be adjusted by an external controller to match varying input speeds, improving robustness to time-scale variations without retraining the network. This approach enables the network to be trained only once at a nominal temporal scale, after which the neuron time constants can be reprogrammed through the nvCAP to shift the network's effective time scale and maintain performance across varying input speeds without retraining.

## 4.2 Refractory Period

The nvCAP can also be used to adjust the refractory period by controlling the magnitude of $C_{rf}$, which is connected to the comparator output (Fig. 3). In the proposed neuron design, the duration of the comparator's high output corresponds to the time during which the neuron is discharging and $V_{mem}$ is held at 0 V. When $C_{rf}$ is in the off-state, the membrane is held at 0 V for a shorter duration compared to when the nvCAP is in the on-state. Increasing the capacitance of the comparator output prolongs the high-output period, thereby holding $V_{mem}$ at 0 V longer and preventing additional spikes or integration during this time.




(a)




(b)

**Figure 5: Speed-adaptation experiment on the UCI-HAR dataset demonstrating time-scale adaptation enabled by the nvCAP-based programmable neuron. (a) Test classification accuracy versus input speed factor. A conventional SNN with fixed membrane time constant shows decreasing accuracy as input speed deviates from the training condition, whereas the programmable neuron maintains nearly constant performance. (b) Selected membrane time constant $\tau$ versus input speed factor. The neuron time constant is dynamically adjusted with input speed by reprogramming the nvCAP membrane capacitor, preserving the effective temporal integration dynamics.**

### 4.3 Synaptic Strength

The third application of the nvCAP device is in controlling the size of the output charge packets. The output charge packet magnitude is determined by the size of the output capacitor $C_{\text{pkt}}$. In this implementation, the synapse is realized using an nvCAP device that is precharged by a voltage source when the neuron is not firing (Fig. 3). The capacitance of this synaptic nvCAP can be dynamically programmed, allowing the connection strength between a presynaptic neuron and its downstream postsynaptic neurons to be adjusted on demand. A higher-capacitance (on-state) nvCAP generates larger charge packets and thus is more likely to induce the postsynaptic neuron to fire. Conversely, an off-state nvCAP produces smaller charge packets and exerts a weaker synaptic effect. If a firing event occurs before the precharge phase is complete, the capacitor releases the available stored charge, resulting in a reduced-amplitude output spike rather than a missed event. This behavior effectively introduces a short-term synaptic depression mechanism under high firing rates [20].

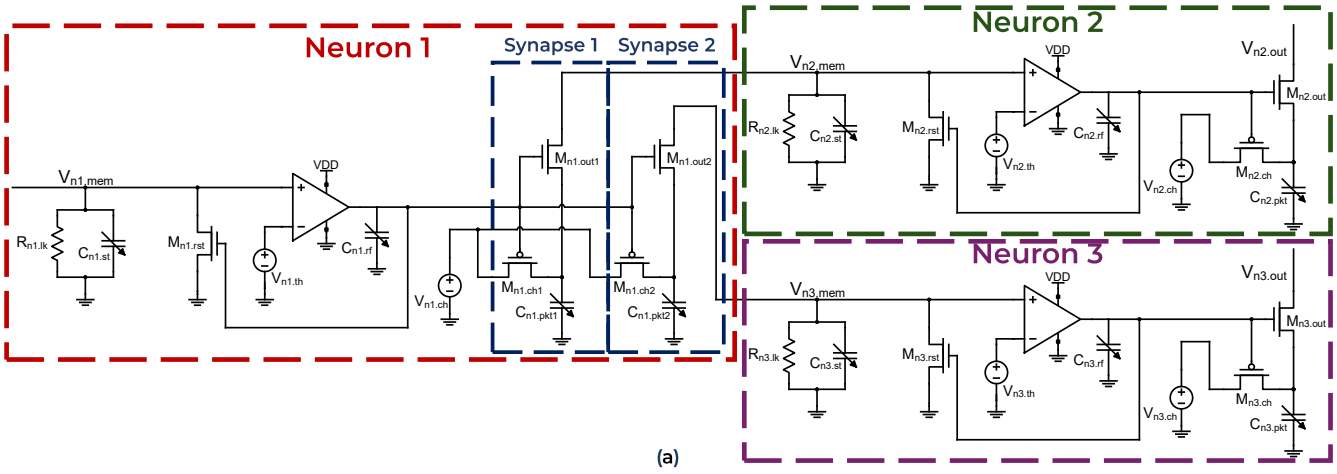
Fig. 6a shows a schematic of one presynaptic neuron with two identical postsynaptic neurons. When both output synapses are programmed to the same state, they release equal-size charge packets; for example, two 500 fF on-state nvCAPs deliver 182 fJ to the downstream neurons. When the synapses are instead programmed to opposite states, they produce charge packets of different magnitudes. For instance, nvCAPs with an on-state of 1.25 pF and an off-state of 50 fF deliver 416.12 fJ and 23.04 fJ, respectively. Fig. 6b illustrates the effect of this unequal weighting: in the simulation, $C_{\text{n1.pkt1}}$ is programmed to the on-state (1.25 pF), while $C_{\text{n1.pkt2}}$ is programmed to the off-state (50 fF) for an on/off ratio of 25. As a result, Neuron 2 receives a larger charge packet, reaches its membrane threshold, and fires, while Neuron 3 receives insufficient charge and remains subthreshold. This ability to precisely weight output charge packets demonstrates the strong potential of nvCAP-based synapses for implementing dynamic, programmable connectivity in neuromorphic circuits.

## 5 Robustness to Non-idealities

The simulations presented above use experimentally calibrated nvCAP models derived from measured device characteristics, but do not capture stochastic and device-to-device non-idealities such as process variation and transient noise. To assess robustness, we therefore perform an additional study in which the neuron is evaluated under nvCAP process variation and transient noise separately.

### 5.1 nvCAP Process Variation

In the previous sections, we demonstrated that tuning the nvCAP capacitance directly modulates the membrane decay time in the speed-adaptable SNN case study. In practice, however, nvCAPs exhibit process variation, which may introduce cycle-to-cycle and device-to-device variability in the programmed on-state capacitance. To assess its effect on neuron operation, we first consider a 5% capacitance variation as a stress-case condition beyond reported values. Under this setting, Monte Carlo simulations show variations in membrane voltage trajectories that lead to occasional differences in output spike trains, as shown in Fig. 7a. We then evaluate the maximum reported nvCAP variability of 3% [15], where simulations show consistent output spike patterns, indicating stable neuron operation under realistic conditions. These results indicate that the proposed neuron remains robust under realistic process variation while maintaining acceptable behavior under more extreme conditions.



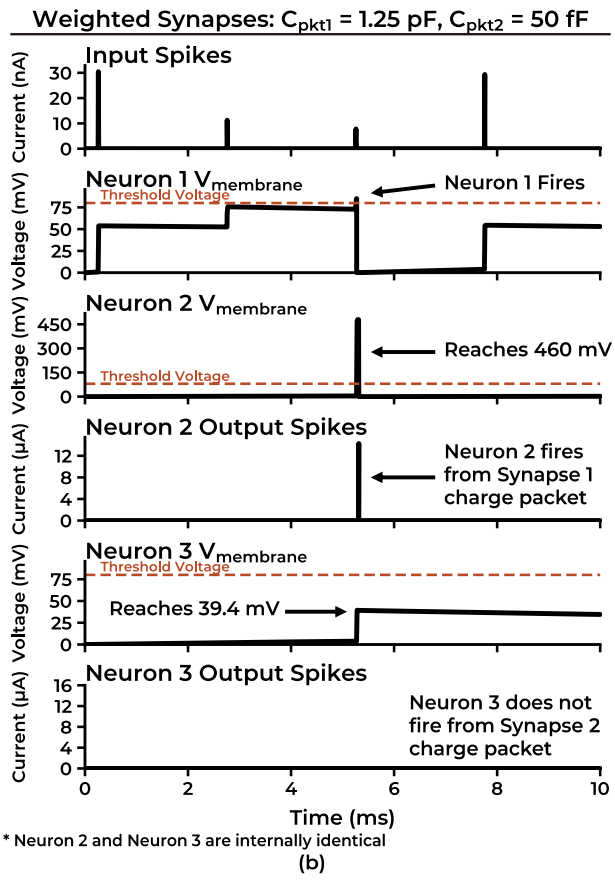




**Figure 6: One-to-two neuron fan-out. Neuron 1 sends weighted charge packets to Neurons 2 and 3 in parallel. (a) Circuit schematic with nvCAP synapses. (b) Effect on identical downstream neurons: Neuron 2 crosses threshold and fires, while Neuron 3 remains subthreshold.**

## 5.2 Transient Noise

To evaluate the impact of noise, we incorporate transient SPICE noise, including thermal, shot, and flicker components. This noise perturbs the comparator sense margin, introducing a sensing delay that temporally spreads the output spikes, as shown in Fig. 7b. This delay can cause spikes arriving during the affected interval to be missed, potentially impacting overall circuit operation. Higher noise frequencies increase the occurrence of this delay. The resulting randomness in spike timing due to these non-idealities could be leveraged for stochastic learning algorithms such as probabilistic spike-timing-dependent plasticity (STDP) [17].

# 6 Benchmarking

To place the proposed neuron in context with prior work, we benchmark its performance against existing implementations. Because the proposed neuron provides multiple tunable parameters, a fixed operating point is selected for fair benchmarking. The selected nvCAP values correspond to a moderate operating point within the achievable design space. While prior simulations demonstrated functionality at larger capacitances and longer timescales, the values used here are chosen to represent a mid-range regime that balances temporal dynamics, energy, and area for consistent comparison. This operating point uses the on-state membrane capacitance $C_{\mathrm{st}} = 100\,\mathrm{fF}$, with leakage resistance $R_{\mathrm{lk}} = 100\,\mathrm{G\Omega}$, threshold $V_{\mathrm{th}} = 80\,\mathrm{mV}$, refractory capacitance $C_{\mathrm{rf}} = 10\,\mathrm{fF}$ (on-state), and a single output packet capacitor $C_{\mathrm{pkt}} = 20\,\mathrm{fF}$ (on-state). These parameters define a representative operating regime enabled by nvCAP programmability.

Consistent with previous approaches, and motivated by relatively high energy consumption during active communication, we evaluate the *energy per spike*, defined as the energy required to generate a single output action potential. At this operating point, circuit simulations yield an energy per spike of 32.32 fJ. This value is parameter-dependent, increasing with larger capacitances or higher threshold voltages. Notably, the definition of energy per spike varies across prior work; here, it includes the energy required to generate weighted output charge packets, whereas some works report only the energy to produce an unweighted spike.

In this case, 87.56% of the energy is consumed by the comparator, with the remainder associated with charging and maintaining the output packet capacitor prior to spike generation. Energy associated with charge injection at the membrane node is not included, as it corresponds to the output activity of the preceding neuron. The estimated layout area per neuron, including one output $C_{\text{pkt}}$, is 69.07 $\mu$m$^2$, demonstrating a compact implementation despite the inclusion of multiple independently tunable neuron parameters.

Table 1 benchmarks the proposed neuron against representative LIF implementations. Prior CMOS neurons primarily achieve tunability through bias-controlled leak currents, effectively modulating $\tau(R)$ while relying on fixed capacitances or capacitive banks. In contrast, this work enables post-fabrication programmability of $\tau(C)$ through the non-volatile nvCAP device, while $V_{\text{th}}$ is independently tuned via the comparator reference voltage. This decoupled control is significant: resistance-based tuning requires continuous biasing and is sensitive to process and temperature variations, often necessitating high-resolution DACs or bias generation circuits to support per-neuron tuning, which increases system complexity and area overhead. By comparison, capacitance-based tuning provides discrete, non-volatile states with improved stability. Furthermore, independent threshold control allows dynamic adjustment of firing behavior without altering the stored neuron state. As a result, the proposed neuron uniquely combines non-volatile time-constant programmability, dynamic threshold control, and charge-domain operation within a single compact circuit. These capabilities are not jointly realized in prior LIF neuron implementations.

Overall, the proposed neuron provides a balanced trade-off between programmability, energy efficiency, and compactness. While prior works typically optimize a single dimension, such as energy, area, or tunability, they do not simultaneously provide non-volatile time-constant control, independent threshold tuning, and charge-domain operation within a single neuron circuit. The combination of low energy per spike (32.32 fJ), small area (69.07 $\mu$m$^2$), and multi-parameter programmability establishes a clear distinction from both conventional CMOS LIF neurons and emerging device-based implementations.

## 7 Conclusion

The proposed charge-domain leaky integrate-and-fire neuron illustrates how non-volatile capacitors can be used not merely as weight storage elements, but as primitives for shaping neural dynamics and communication. By programming the membrane, reset, and synaptic charge paths in the capacitance domain, this approach decouples neuron behavior from fixed device parameters and opens a richer design space in which temporal constants, firing thresholds, and fan-out strengths become reconfigurable, non-volatile degrees of freedom. Circuit-level evaluation in a 28-nm CMOS process with experimentally calibrated nvCAP models confirms that the proposed neuron supports tunable membrane dynamics, refractory behavior, and synaptic weighting within a compact and energy-efficient implementation. At the system level, a speed-adaptable SNN classification study demonstrates that programmable membrane time constants enable robustness to input time-scale variations, allowing a network trained at a nominal condition to maintain performance across varying speeds without retraining. Benchmarking against

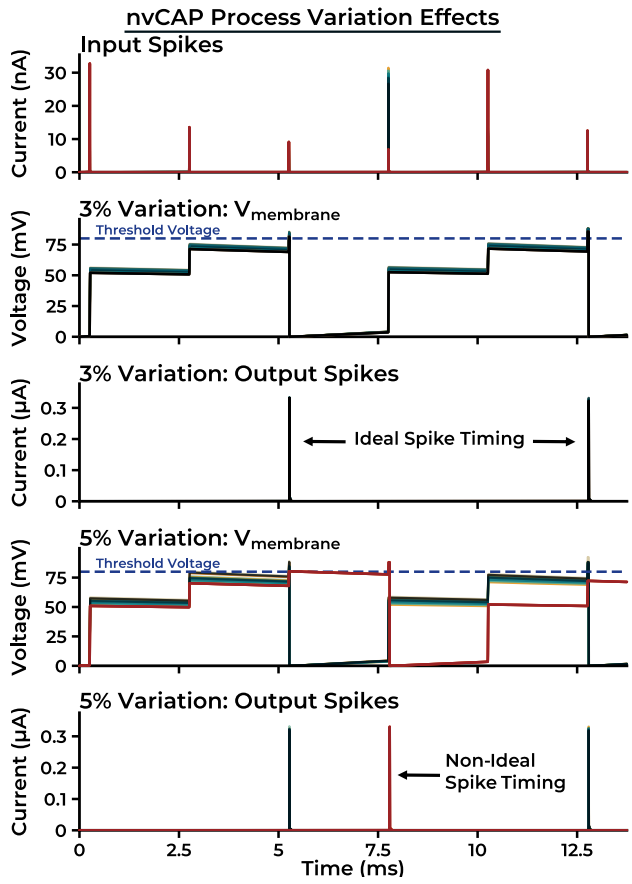



**Figure 7: Circuit robustness study. Each color represents a different simulation run. (a) Monte Carlo simulations with 3% nvCAP variation show consistent output spike patterns, while 5% variations show largely consistent spike trains with occasional deviations (red). (b) Transient noise simulations at 100 kHz show noise-induced comparator delay.**

**Table 1: Benchmarking**

| Publication | Type | Comp. Domain | Post-Fabrication Tunable Params. | NVM | Tech. | VDD | Energy/Spike | Area |
|---|---|---|---|---|---|---|---|---|
| Yang et al., ISLPED (2021) [22] | LIF | Current | Not explicit | No | 55 nm | 1 V | 1.099 nJ | – |
| Indiveri et al., IEEE TNN (2006) [8] | LIF | Current | $V_{\text{th}}$, $\tau_m(R)$, $t_{\text{ref}}$(bias), SFA | No | 0.8 $\mu$m | 3.3 V | 900 pJ | 2573 $\mu$m$^2$ |
| Joubert et al., IJCNN — Digital (2012) [9] | LIF | Voltage | $\tau_m(R)$, $w$ | No | 65 nm | – | 41.3 pJ | 538 $\mu$m$^2$ |
| Dutta et al., Sci. Rep. (2017) [4] | Single-Device LIF | Current | None reported | No | 32 nm PD-SOI | – | 35 pJ | – |
| Joubert et al., IJCNN — Analog (2012) [9] | LIF | Current | $\tau_m(R)$, $w$ | No | 65 nm | – | 2 pJ | 120 $\mu$m$^2$ |
| Sourikopoulos et al., Front. Neurosci. (2017) [19] | LIF | Current | None reported | No | 65 nm | 0.2 V | 4 fJ | 35–200 $\mu$m$^2$ |
| Besrour et al., arXiv (2024) [2] | LIF | Current | $V_{\text{th}}$, $\tau_m(R)$, $t_{\text{ref}}$(bias) | No | 28 nm | 0.25 V | 1.61 fJ | 34 $\mu$m$^2$ |
| Zare et al., Neurocomputing (2021) [24] | LIF | Current | Firing rate (adapt.) | No | 130 nm | 0.5 V | 0.67 fJ | 22 $\mu$m$^2$ |
| Seenivasan et al., Microsyst. Technol. (2025) [18] | LIF | Current | $V_{\text{th}}$, $\tau_m(R)$, $t_{\text{ref}}$(bias) | No | 45 nm | 1 V | 524.415 aJ | – |
| **This work** | **LIF** | **Charge** | $V_{\text{th}}$, $\tau_m(C_{\text{nv}})$, $t_{\text{ref}}$, $w$ | **Yes** | **28 nm** | **1 V** | **32.32 fJ** | **69.07$\mu$m$^2$** |

$\tau_m(R)$: membrane time constant tuned via leak resistance or bias-controlled current. $\tau_m(C_{\text{nv}})$: membrane time constant tuned via non-volatile capacitance. $t_{\text{ref}}$: refractory period. SFA: spike-frequency adaptation. Single-Device LIF: neuron behavior implemented primarily by a single device with minimal supporting circuitry. Energy/Spike values are reported as defined in each cited work and may not be directly comparable.

prior LIF neuron implementations further highlights that the proposed design provides a balanced trade-off between energy, area, and multi-parameter programmability while uniquely combining charge-domain operation with non-volatile neuron tuning.

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